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*Intellectual Property Law* MAY 18 2005

# F A C S I M I L E

Name: U.S. Patent & Trademark Office  
FAX: (703) 872-9306  
Application No.: 10/628,986  
Filing Date: July 28, 2003  
Inventor: WHITEFIELD, Bruce et al.  
Art Unit: 2825  
Examiner: Siek, Vuthe  
From: Eric J. Whitesell, Reg. No. 38,657   
Today's Date: May 18, 2005  
Attorney Docket No.: 03-0593 81577/6653  
Pages: 13 pages (including this 1-page coversheet)  
Dispatched by: Susan R. Telford

**Transmitted herewith for filing via facsimile:**

Transmittal Form (1 pg.); Amendment "A" (11 pgs.); Fax coversheet (1 pg.)

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PTO/SB/21 (04-04)

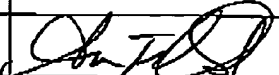
Approved for use through 07/31/2006. OMB 0651-0031

U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE

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<b>Transmittal Form</b> <i>(to be used for all correspondence after initial filing)</i>	Application Number	10/628,986	
	Filing Date	07/28/2003	
	First Named Inventor	WHITEFIELD, Bruce	
	Art Unit	2825	
	Examiner Name	Siek, Vurthe	
Total Number of Pages in This Submission		13	
		Attorney Docket Number	03-0593 81577/6653

ENCLOSURES (CHECK ALL THAT APPLY)		
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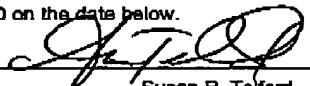
IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant: WHITEFIELD, Bruce  
et al.  
Serial No.: 10/628,986  
Filed: July 28, 2003  
For: METHOD OF MAPPING LOGIC  
FAILURES IN AN INTEGRATED  
CIRCUIT DIE  
Art Unit: 2825  
Examiner: Siek, Vuthe

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RESPONSE TO OFFICE ACTION UNDER 37 C.F.R. § 1.111

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